WHAT IS CLAIMED IS:

1. A semiconductor device having a test mode and a normal mode as operation modes, comprising a test mode control circuit,

said test mode control circuit including:

a first comparing circuit for comparing a reference potential with a test mode setting potential supplied from the outside;

a test setting control unit for generating a test mode entry signal in accordance with an output of said first comparing circuit when said reference potential is lower than a predetermined potential, and generating said test mode entry signal irrespective of an output of said first comparing circuit when said reference potential is at least said predetermined potential; and

a test mode signal outputting circuit for outputting a test mode signal indicative of activation of a predetermined test operation in accordance with an output of said test setting control unit.

2. The semiconductor device according to claim 1, further comprising an internal power supply potential generating circuit for receiving an external power supply potential and generating a stabilized internal power supply potential,

wherein said test setting control unit includes:

a first potential down converting circuit for receiving said reference potential and outputting a potential lower than said reference potential;

an inverter for receiving an output of said potential down converting circuit as an input signal and receiving said internal power supply potential as an operation power supply potential; and

a gate circuit for outputting said test mode entry signal in accordance with an output of said inverter and an output of said first comparing circuit.

3. The semiconductor device according to claim 2, wherein said first potential down converting circuit has a plurality of voltage dividing devices

connected in series between a node for receiving said reference potential and a ground node, and

said inverter receives, as said input signal, one of potentials of the connecting nodes of said plurality of voltage dividing devices.

4. The semiconductor device according to claim 2, wherein said first potential down converting circuit has a plurality of field effect transistors which are connected in series so as to form diodes between a node for receiving said reference potential and a ground node,

each of said plurality of field effect transistors has a back gate connected to a source, and

said inverter receives, as said input signal, a potential of one of the connecting nodes of said plurality of field effect transistors.

5. The semiconductor device according to claim 2, wherein said reference potential is equal to said external power supply potential.

6. The semiconductor device according to claim 1, further comprising an internal power supply potential generating circuit for receiving an external power supply potential and generating a stabilized internal power supply potential,

wherein said test setting control unit has

a first potential down converting circuit for receiving said reference potential and outputting a potential lower than said reference potential;

a second potential down converting circuit for receiving said internal power supply potential and outputting a potential lower than said internal power supply potential;

a second comparing circuit for comparing outputs of said first and second potential down converting circuits; and

a gate circuit for outputting said test mode entry signal in accordance with outputs of said first and second comparing circuits.

7. The semiconductor device according to claim 6, wherein said first

potential down converting circuit has a plurality of first voltage dividing devices connected in series between a node for receiving said reference potential and a ground node,

said second potential down converting circuit has a plurality of second voltage dividing devices connected in series between a node for receiving said internal power supply potential and a ground node, and

said second comparing circuit compares a potential of one of the connecting nodes of said plurality of first voltage dividing devices and a potential of one of the connecting nodes of said plurality of second voltage dividing devices.

8. The semiconductor device according to claim 6, wherein said first potential down converting circuit has a plurality of first field effect transistors connected in series so as to form diodes between a node for receiving said reference potential and a ground node,

each of said plurality of field effect transistors has a back gate connected to a source,

said second potential down converting circuit has a plurality of second field effect transistors connected in series so as to form diodes between a node for receiving said internal power supply potential and the ground node,

each of said plurality of second field effect transistors has a back gate connected to a source, and

said second comparing circuit compares a potential of one of the connecting nodes of said plurality of first field effect transistors and a potential of one of the connecting nodes of said plurality of second field effect transistors.

9. The semiconductor device according to claim 6, wherein said reference potential is equal to said external power supply potential.

10. The semiconductor device according to claim 1, further comprising:

a memory array including a plurality of memory cells arranged in a matrix;

a row selecting circuit for selecting a row of said memory cells in accordance with an address signal; and

a column selecting circuit for selecting a column of said memory cells in accordance with said address signal,

said test mode output circuit having a gate circuit for decoding said address signal and outputting said test mode signal when said test entry signal is activated.